

The schematic diagram illustrates a unit cell array region of a semiconductor device. It features a grid of four rectangular unit cells arranged in two rows and two columns. Each unit cell contains three main components: a central square element labeled 113a, a larger rectangular element labeled 102b positioned below it, and another rectangular element labeled 102a located to the right of 102b. The elements are interconnected by a network of horizontal and vertical lines representing electrical connections. Dashed lines indicate specific regions or boundaries within each unit cell. Labels 118c and 131a are used to denote specific areas or layers at the top and bottom of the array, respectively. Arrows labeled I and II point towards the central elements 113a and 102b, while arrows labeled I' and II' point towards the outer edges of the unit cells.

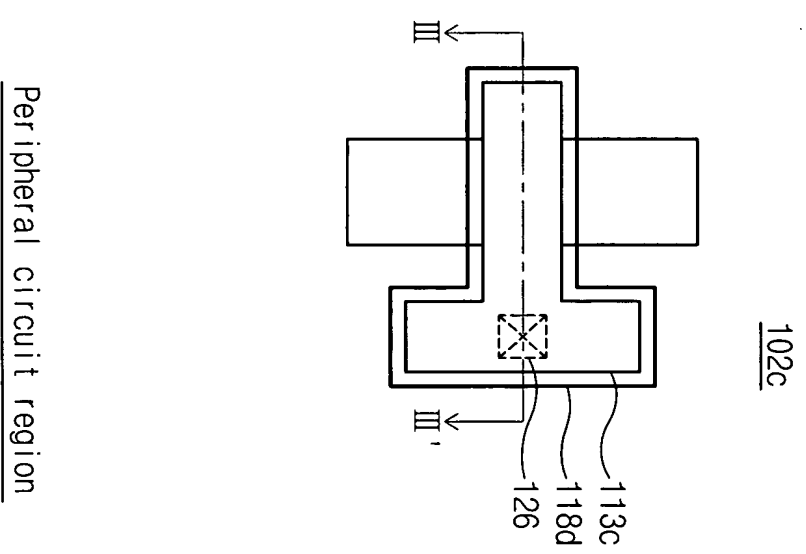


Fig. 2

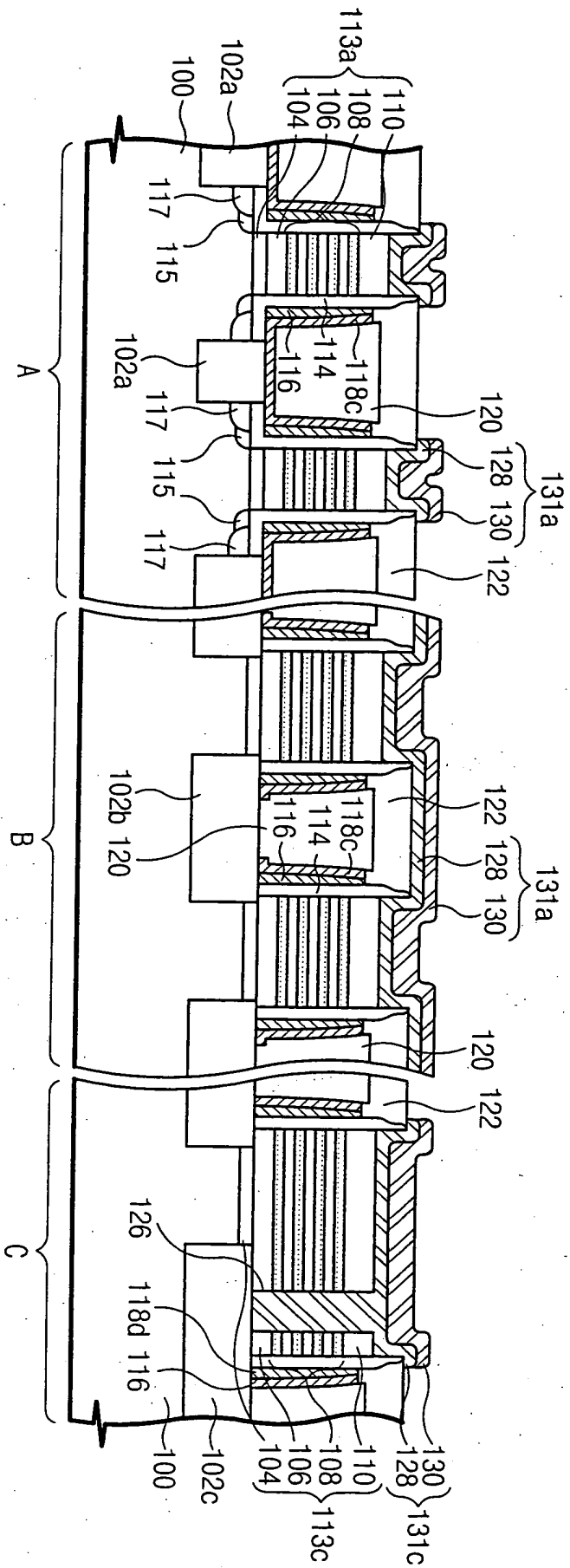


Fig. 3A

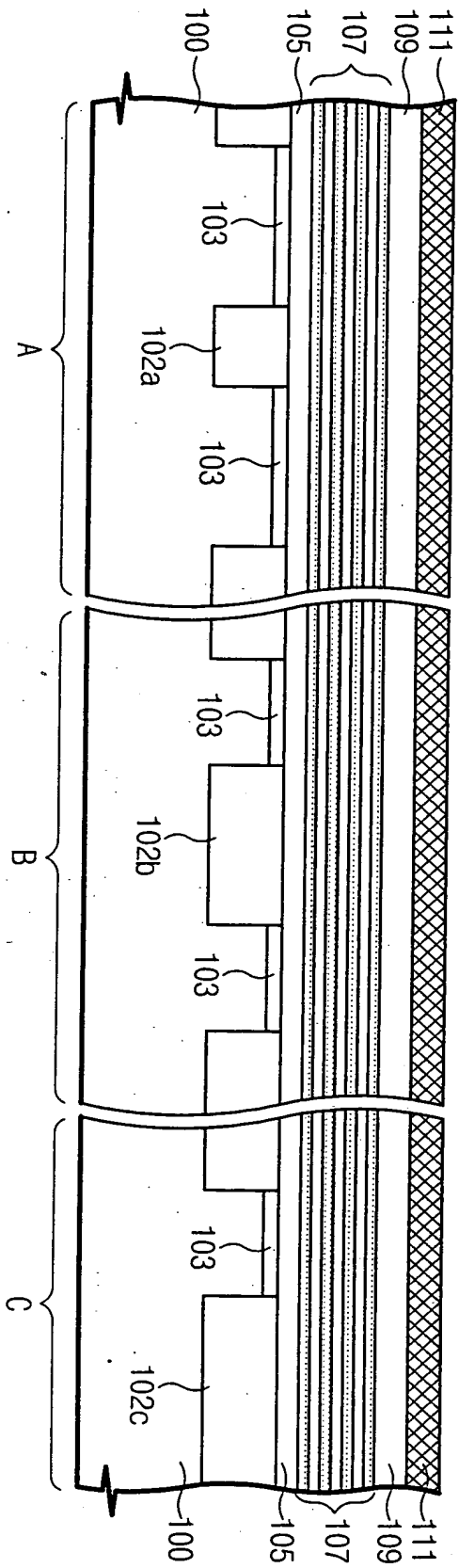


Fig. 3B

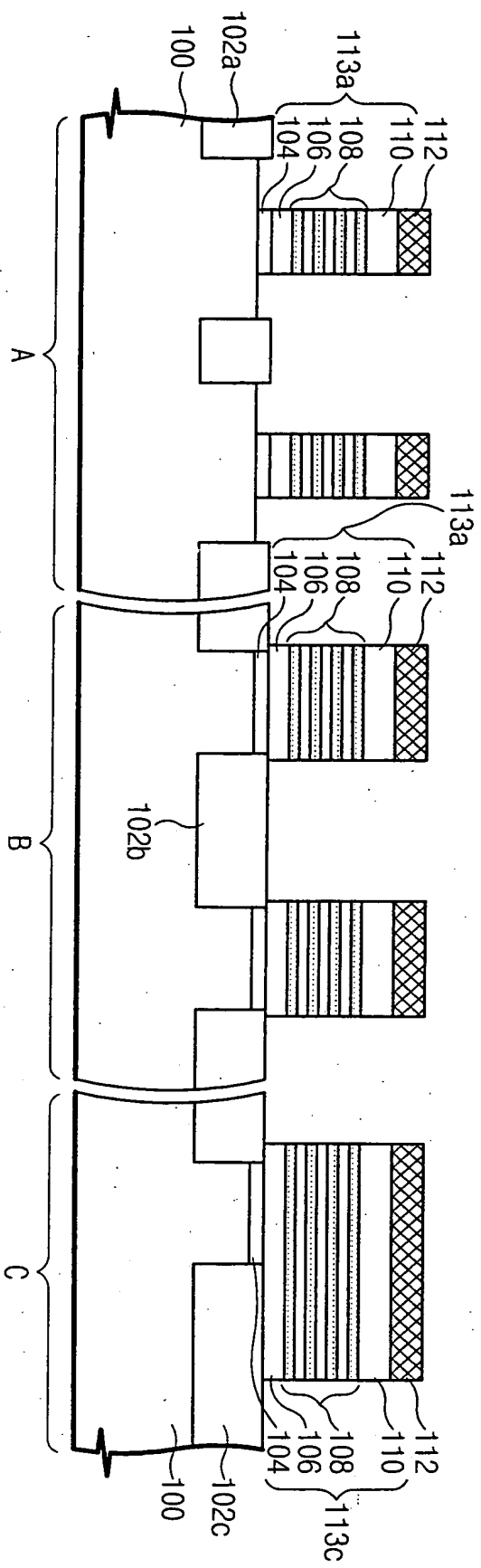


Fig. 3C

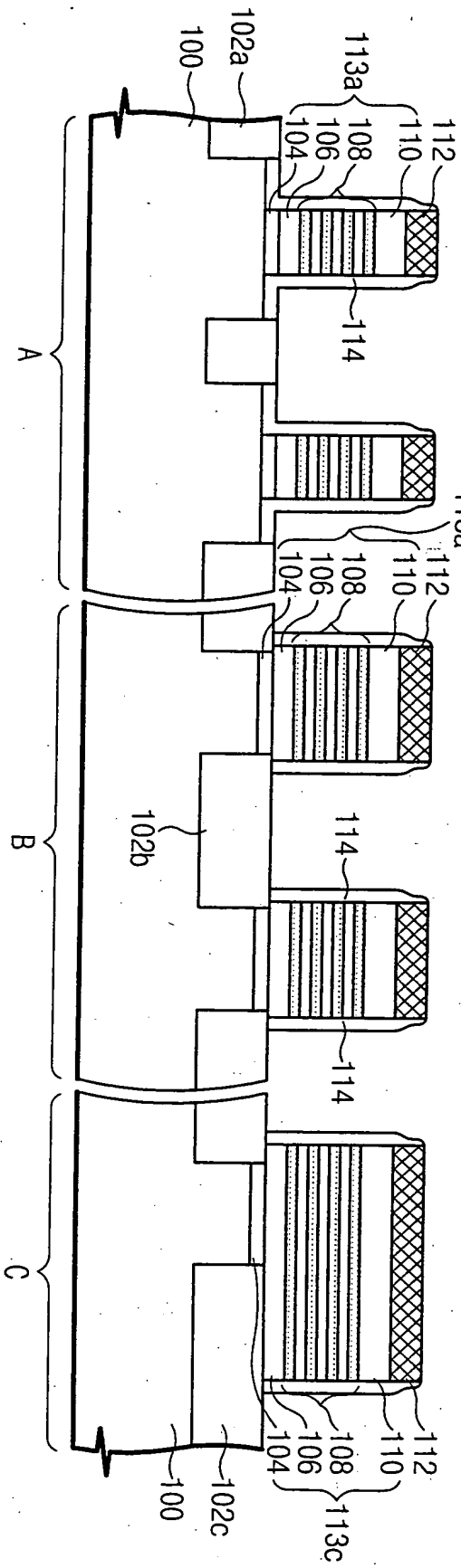


Fig. 3D

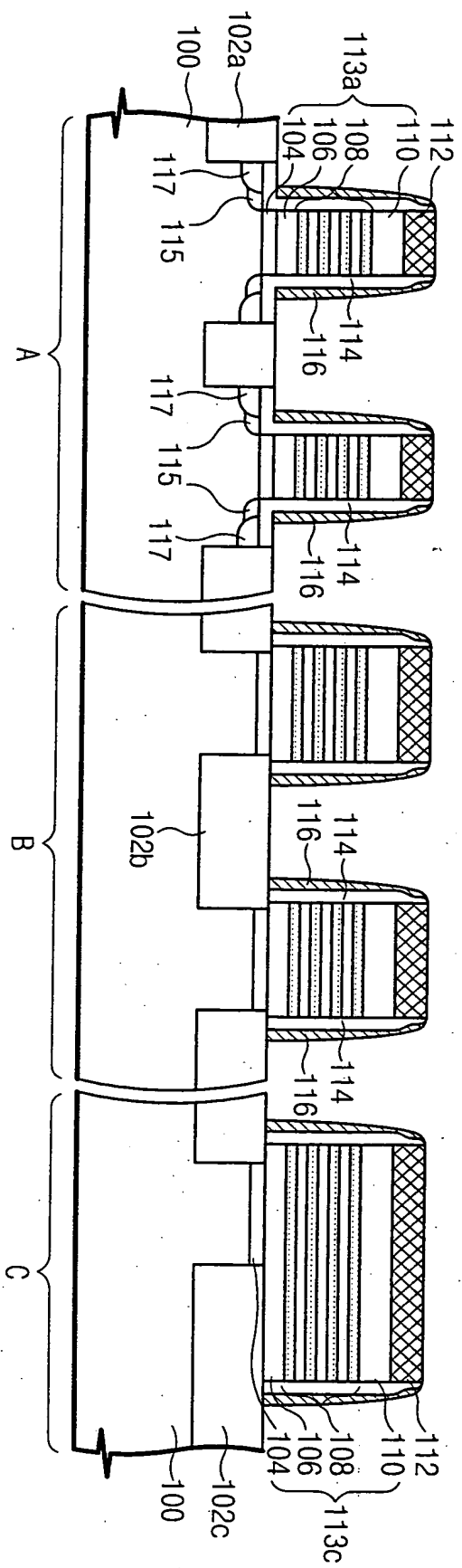


Fig. 3E

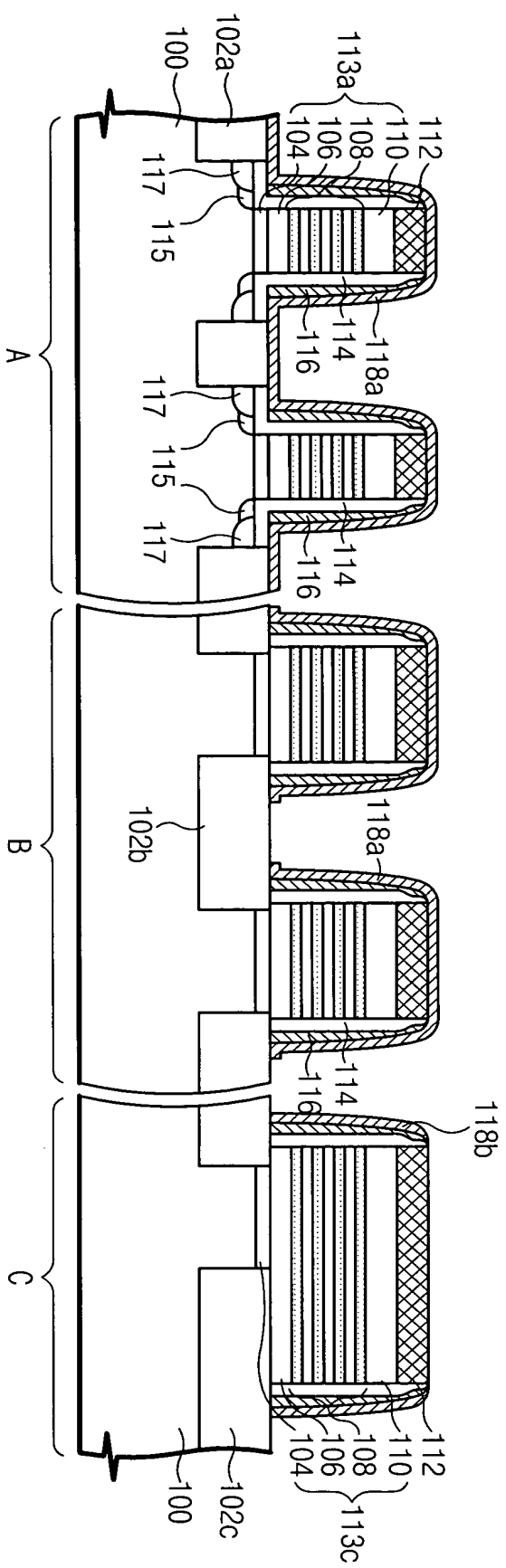


Fig. 3F

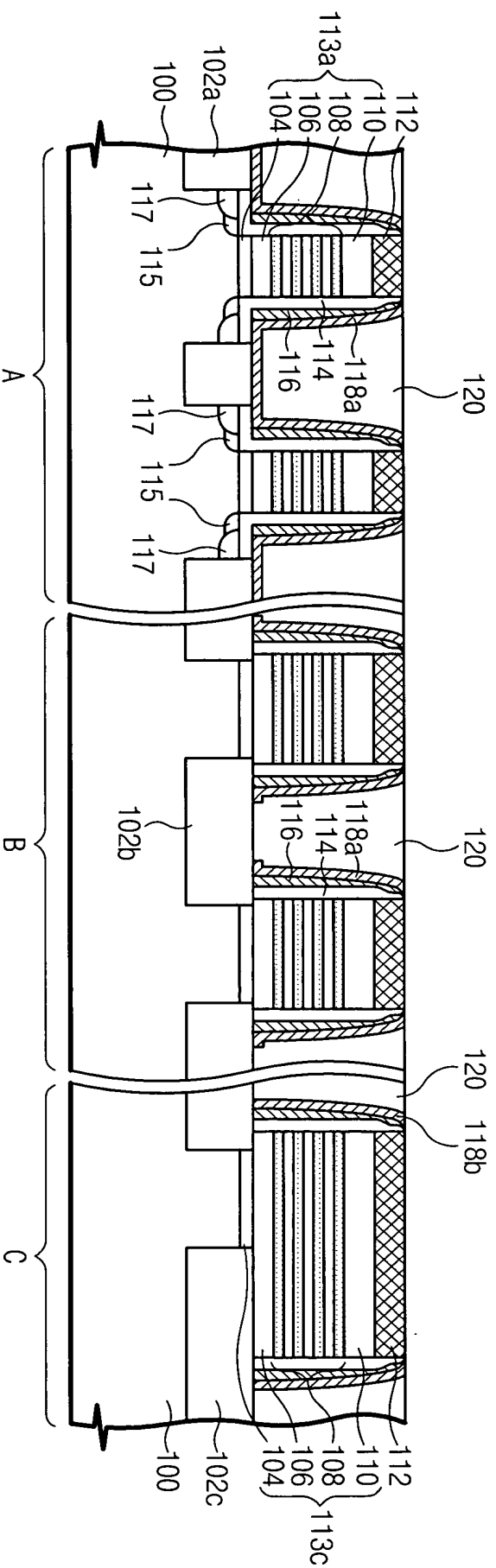




Fig. 3G

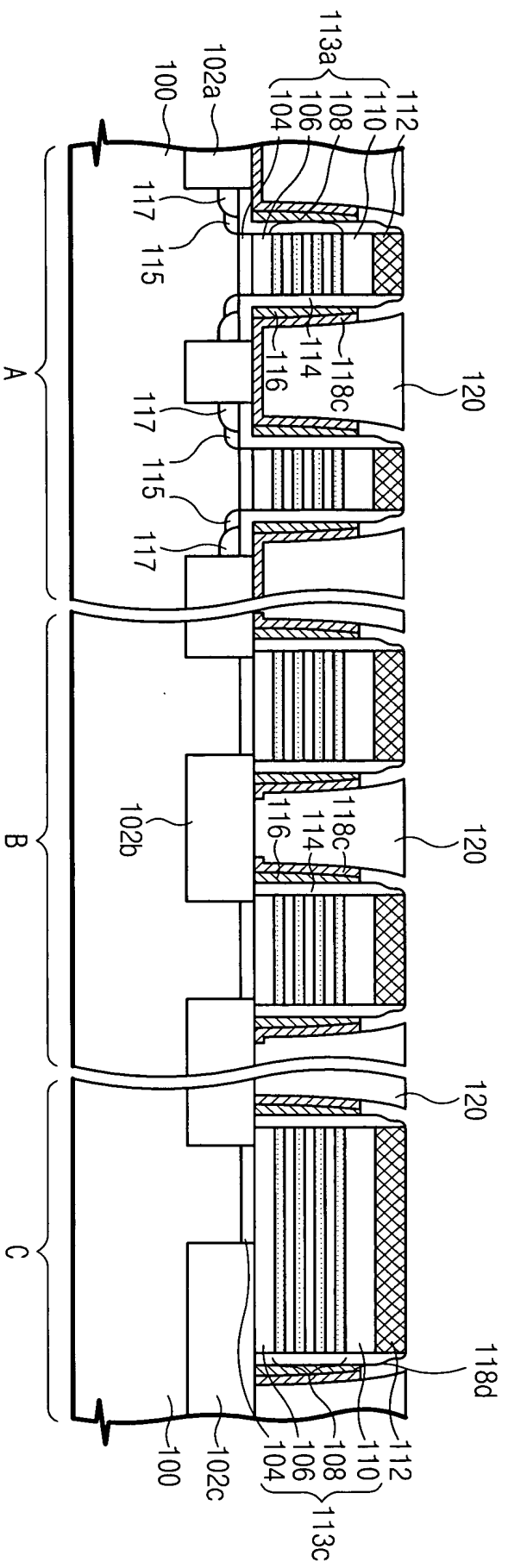


Fig. 3H

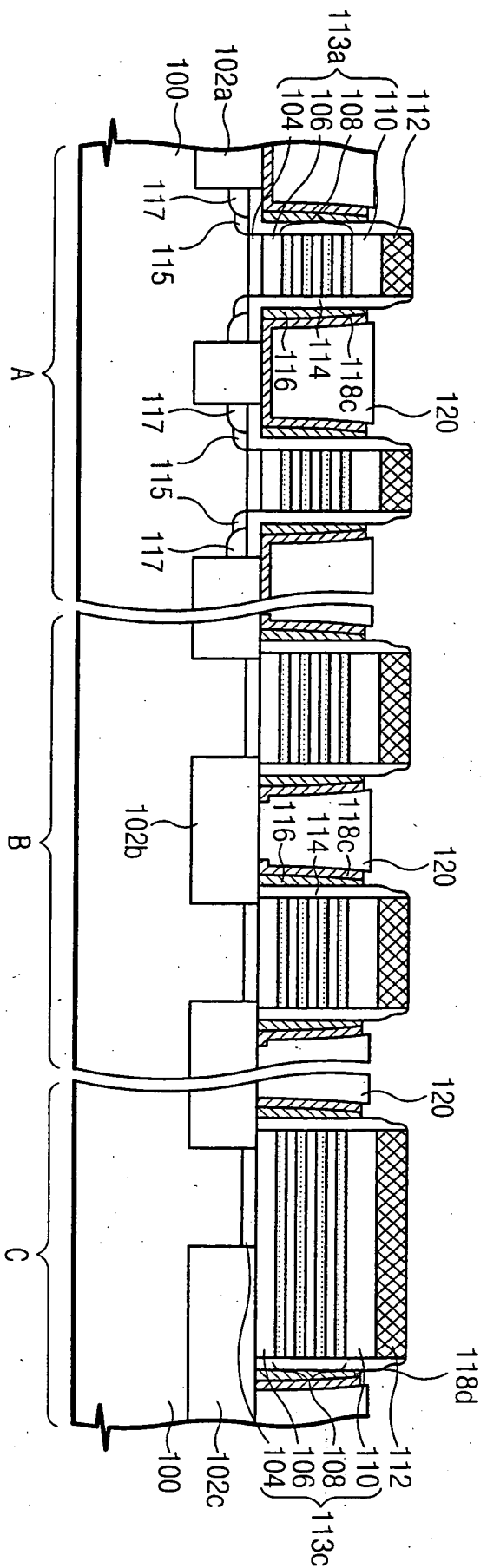




Fig. 3J

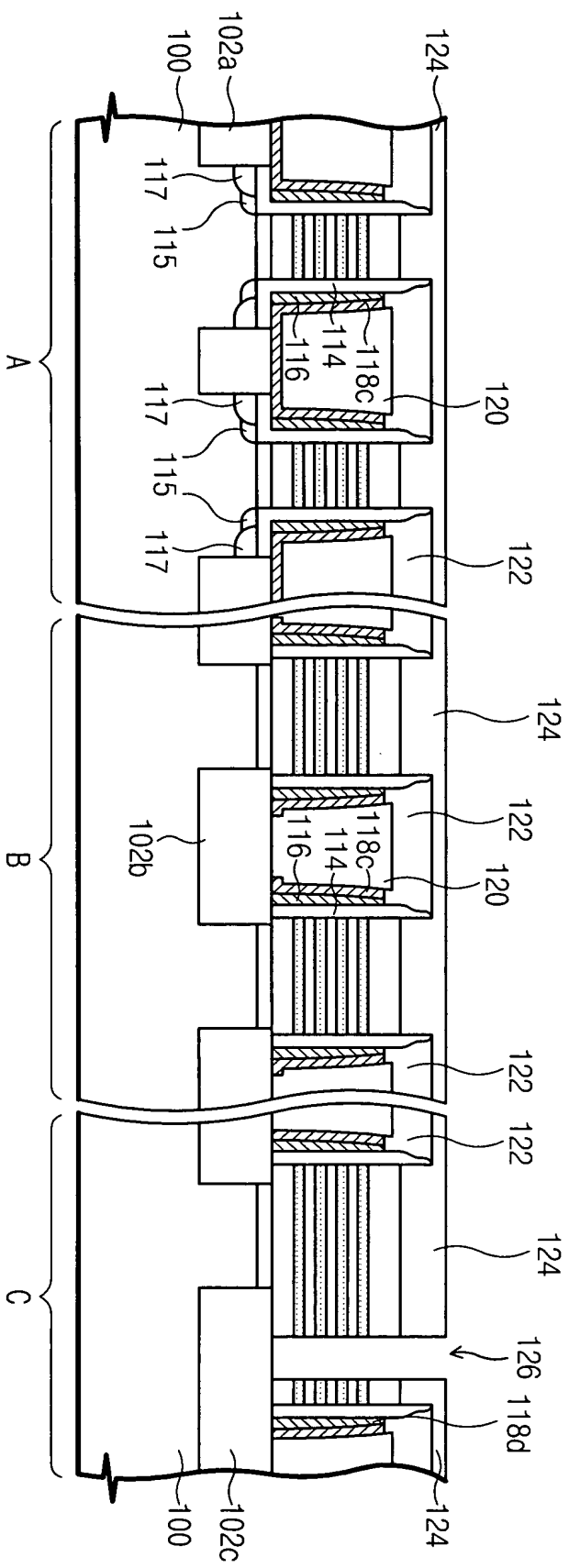


Fig. 3K

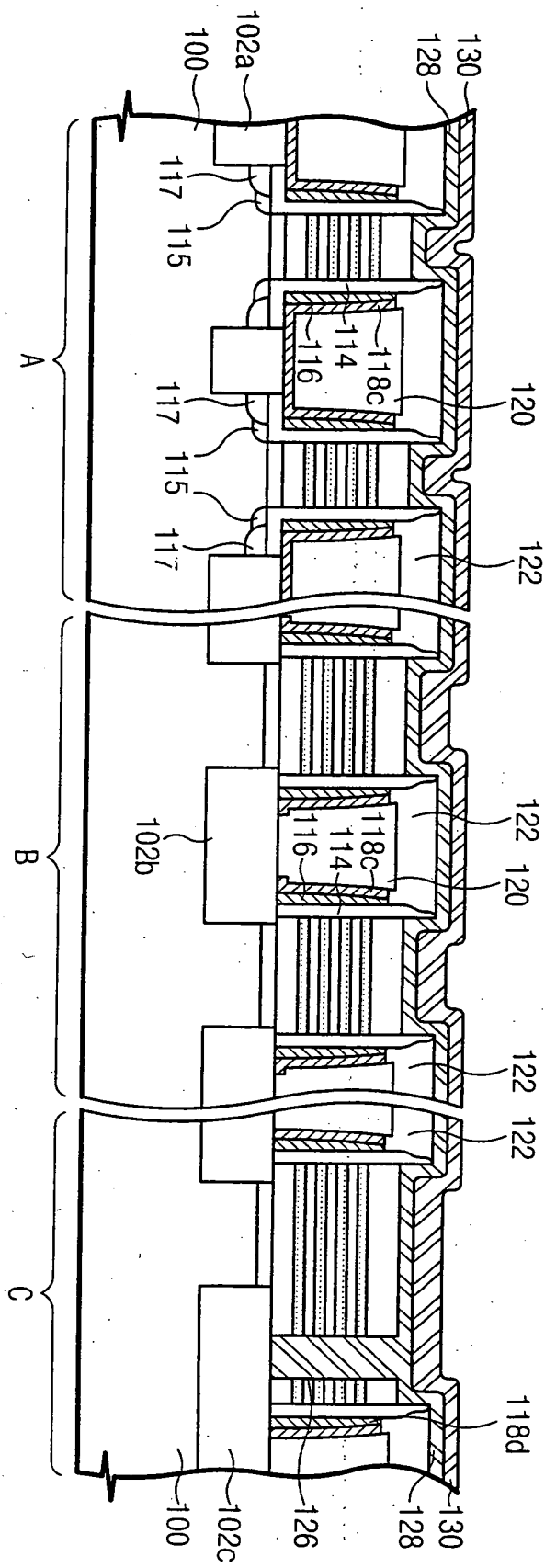


Fig. 4

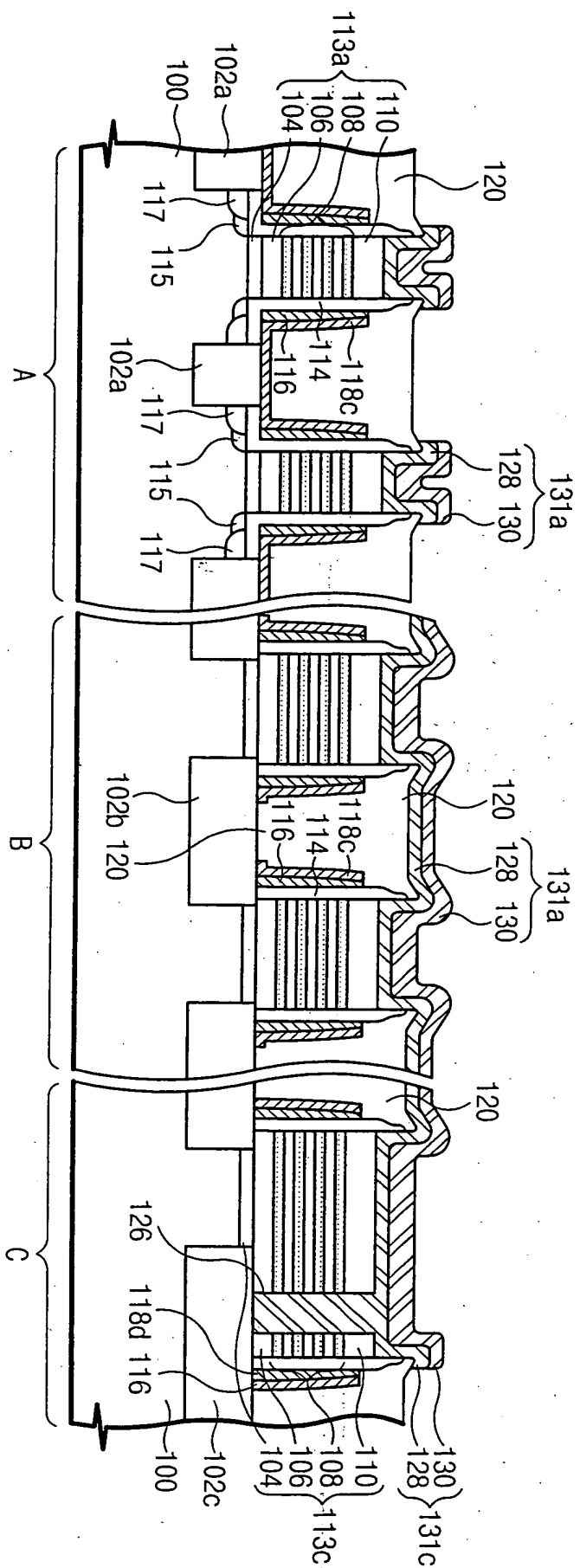


Fig. 5

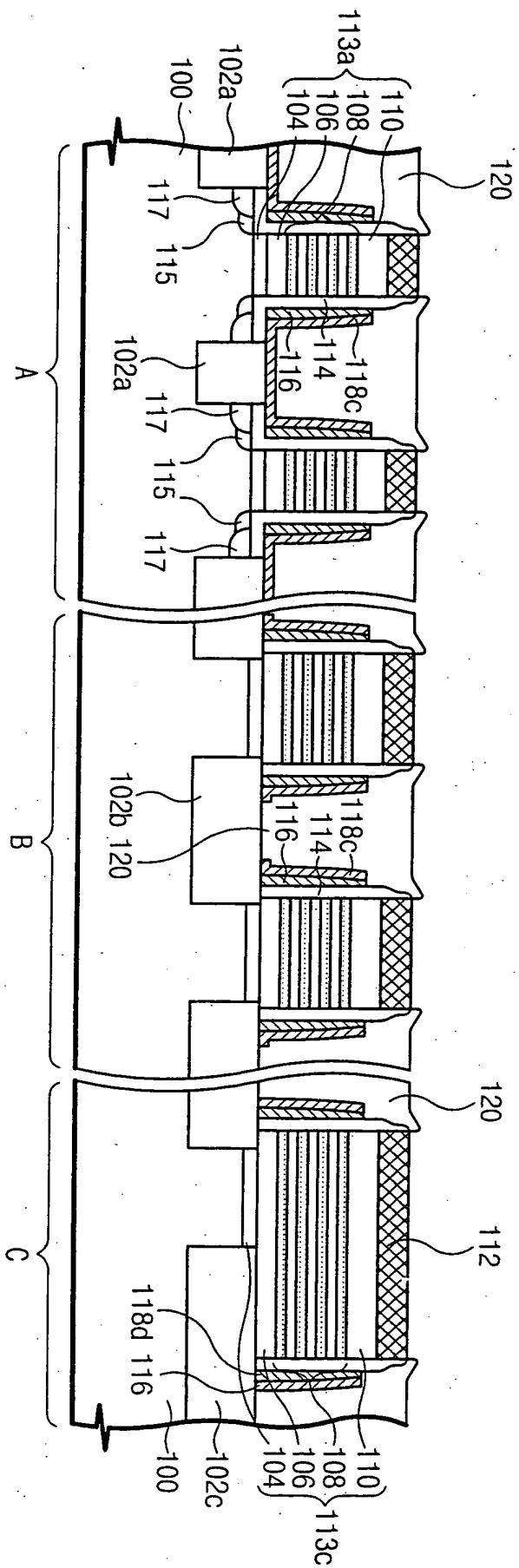


Fig. 6

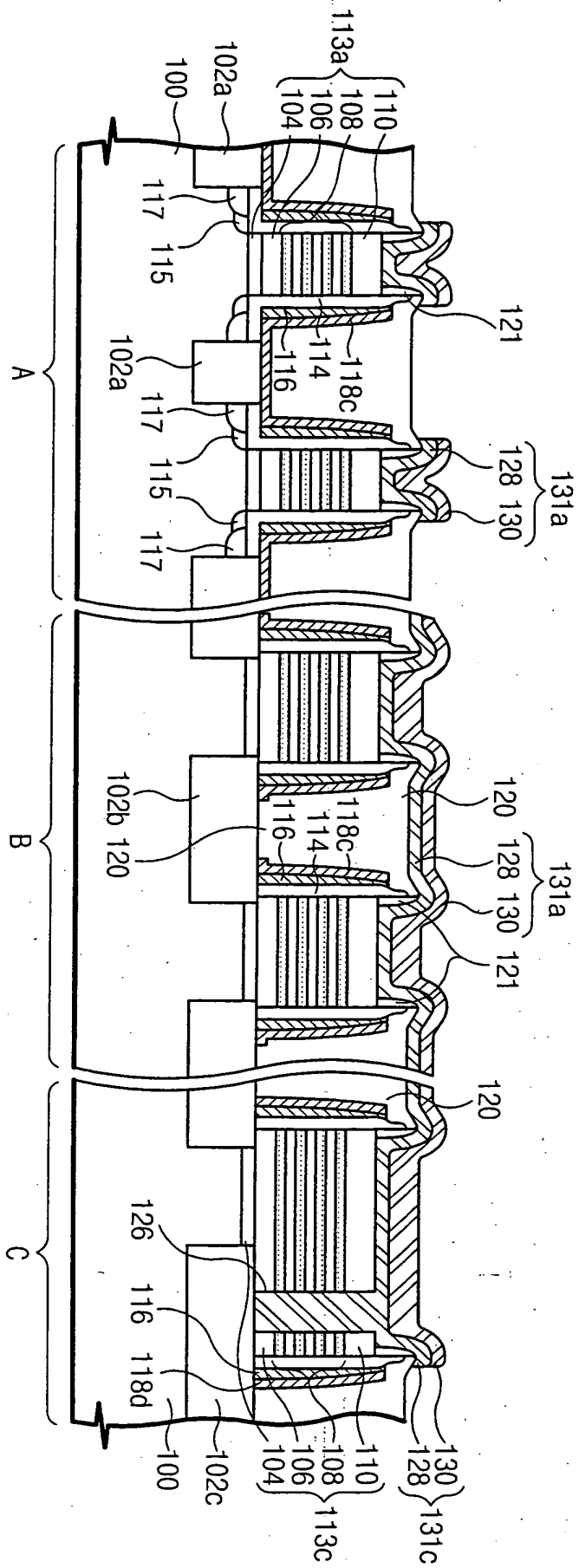




Fig. 7

